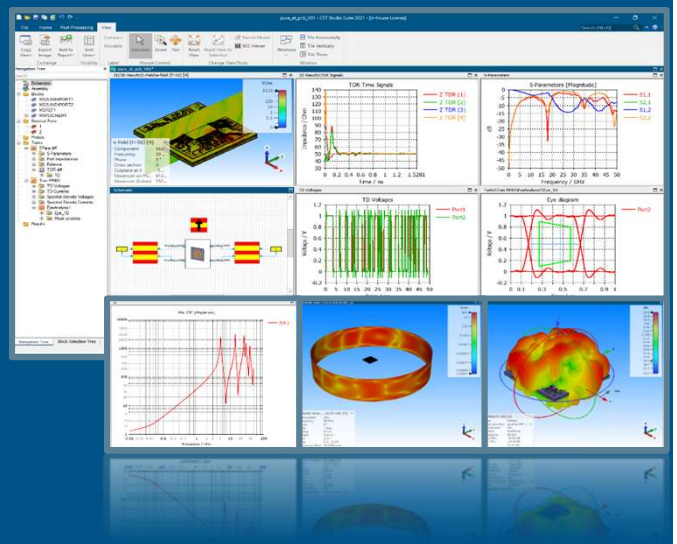
3DEXPERIENCE®

SIMULIA EMAG SOLUTION

SI-PI-EMC-Thermal

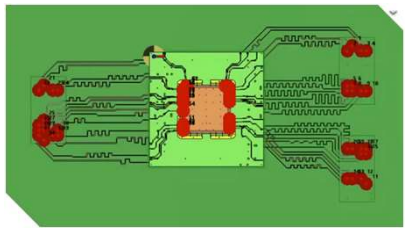


DASSAULT SYSTEMES | The 3DEXPERIENCE® Company

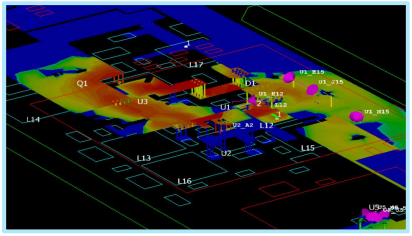
Connected to **3D experience platform**

CST STUDIO SUITE 2023
SIMULIA Electromagnetic solution

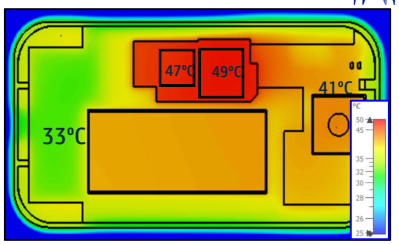
Signal Integrity



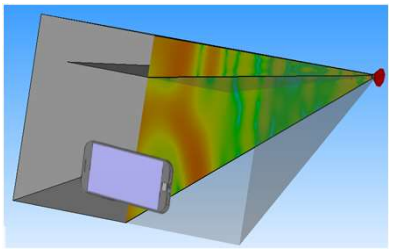
Power Integrity



Thermal Integrity



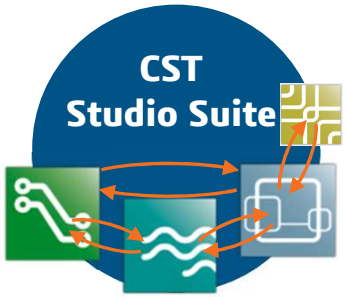
EMC



SIMULIA

DASSAULT SYSTEMES

CST Ecosystem

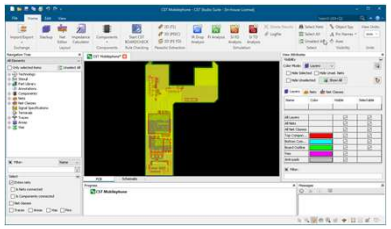


Tightly linkage between CST products.

CST PCB Studio

For signal and power integrity analysis of PCBs

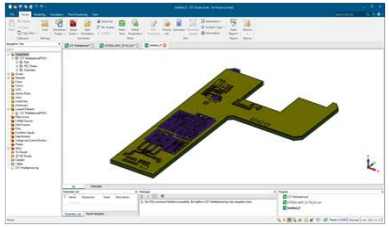
- PCB import
- Impedance calculator
- Component handling
- Rule based checking (SI/PI/EMC)
- Spezialized solver technology:
  - 2DTL, PEEC, FEFD (3D)
- Convenient workflows:
  - IR-Drop / SI (TD & FD) / PI / DDR4
  - DeCap optimization



CST Microwave Studio

3D EM Simulation for high frequencies

- High accuracy fullwave EM 3D solver
  - Time Domain, Frequency Domain
- Tetrahedral & Hexahedral Meshing
- Visualization of fields
- Post-Processing



CST MPHYSICS Studio

For thermal analysis of PCBs and Components.

- Specialized EDA import
- Coupled workflows EM – Thermal
- Solvers:

CST Design Studio

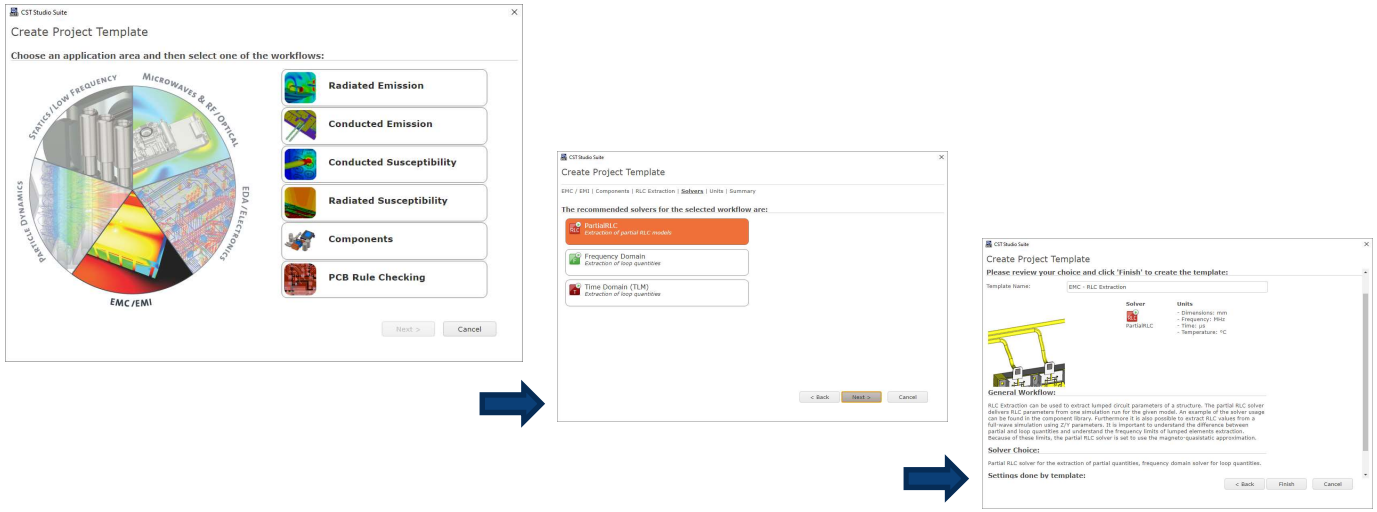
For circuit co-simulation and synthesis

- Circuit simulator (Spice)
- Data import (Spice, TS, IBIS,...)
- Configurable blocks
  - Ideal TL, microstrip, stripline, ...
- Circuit elements
  - Passive / active models, sources, ..
- Simulation tasks:
  - S-Parameter, Transient, AC-Task, ...
- Control tasks:
  - Parameter Sweep, Optimization, Post-Processing

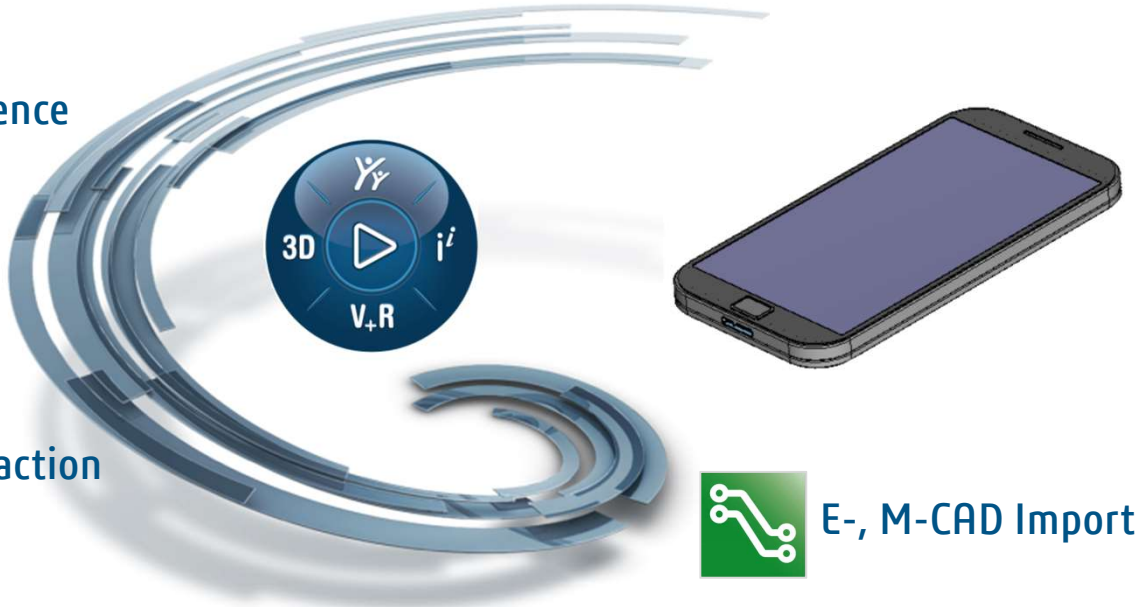
Solver from DC to THz

PROJECT TEMPLATE SELECTION

- Project Templates have been available for many years
- Highly recommended to use them
  - Propose best solver,
  - Set up units, boundary conditions, mesh settings, solver settings, monitors, probes
- A major update of EMC project templates in CST Studio Suite ® 2023.



CST Simulation Workflows Overview



Thermal Simulation

RF Interference

EMC - PDN
Conducted Emission
Radiated Emission

Partial RLC Extraction

E-, M-CAD Import

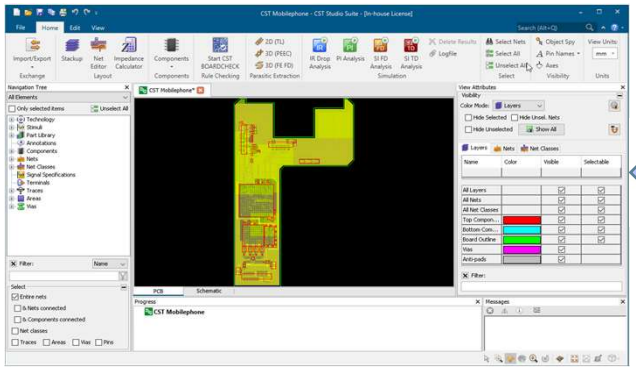
Signal Integrity

Power Integrity

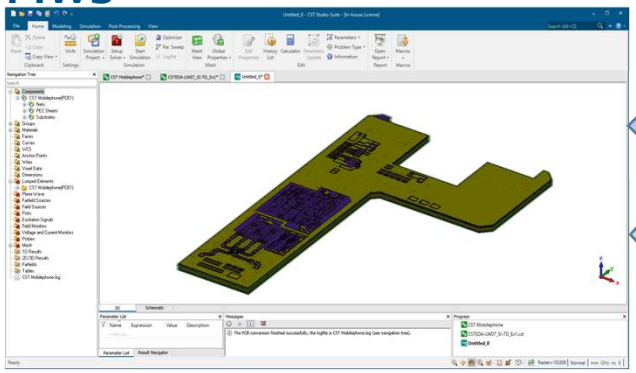
DASSAULT SYSTEMES

GEOMETRY IMPORT

PCBS

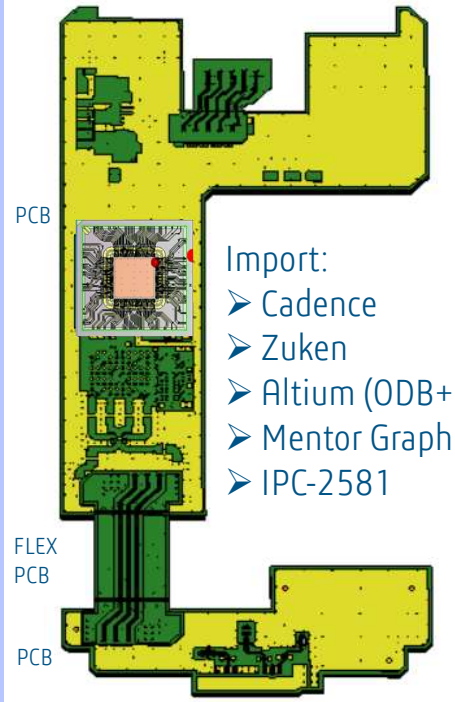


MWS



E-CAD

EDA Import



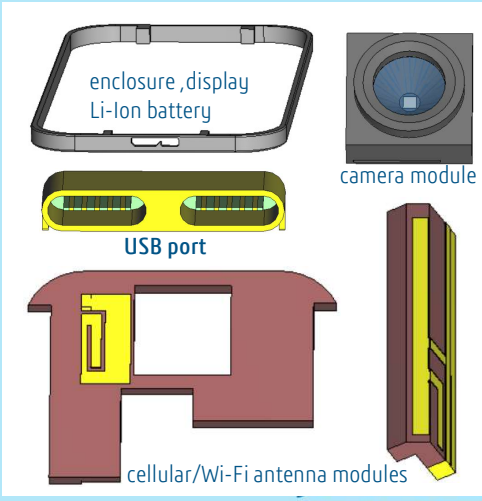
Import:

- Cadence
- Zuken
- Altium (ODB++)
- Mentor Graphics
- IPC-2581

M-CAD

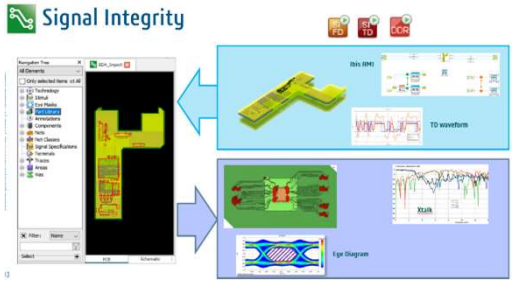
3D Import

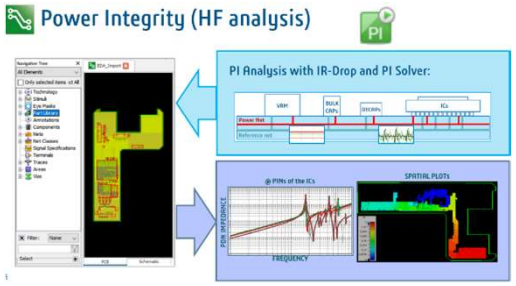
- CATIA
- SOLIDWORKS
- Autodesk
- PT Creo
- Siemens NX
- STEP
- STL
- IGES
- OBJ
- NASTRAN

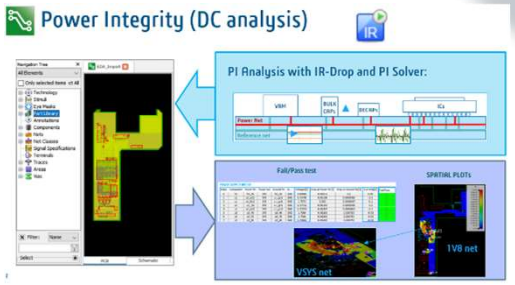


SIMULIA

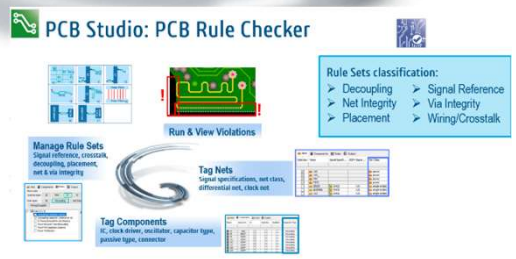
PCB Studio GUI for automated and dedicated analysis

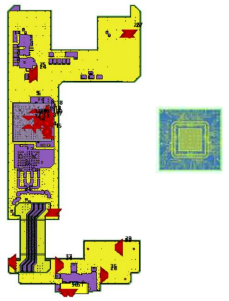






CST Studio Suite 2023

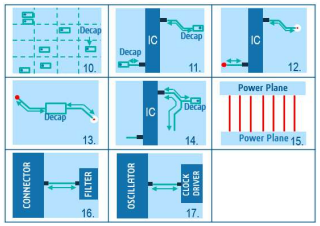


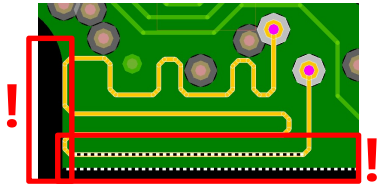


CPU or PCB import in PCB Studio GUI

PCB Studio: PCB Rule Checker

Goal: PCB layout assessment





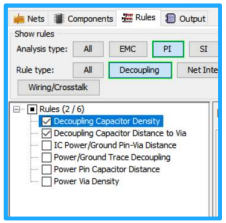
Run & View Violations

Rule Sets classification:

- Decoupling
- Net Integrity
- Placement
- Signal Reference
- Via Integrity
- Wiring/Crosstalk

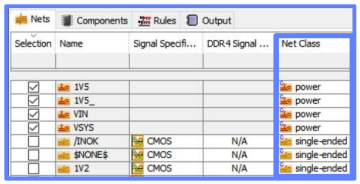
Manage Rule Sets

Signal reference, crosstalk, decoupling, placement, net & via integrity



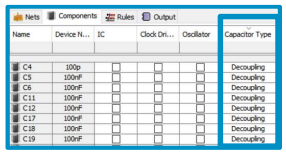
Tag Nets

Signal specifications, net class, differential net, clock net

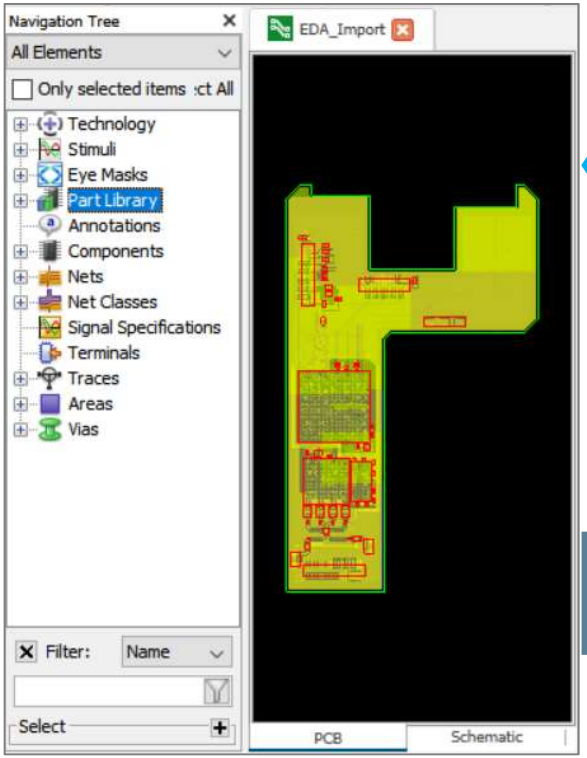


Tag Components

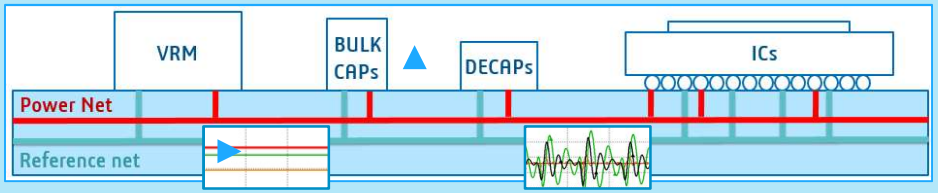
IC, clock driver, oscillator, capacitor type, passive type, connector



Power Integrity (DC analysis)



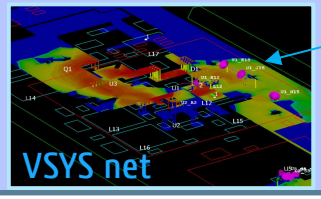
PI Analysis with IR-Drop and PI Solver:



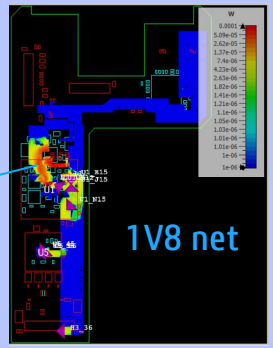
Fail/Pass test

POWER SUPPLY AND IO

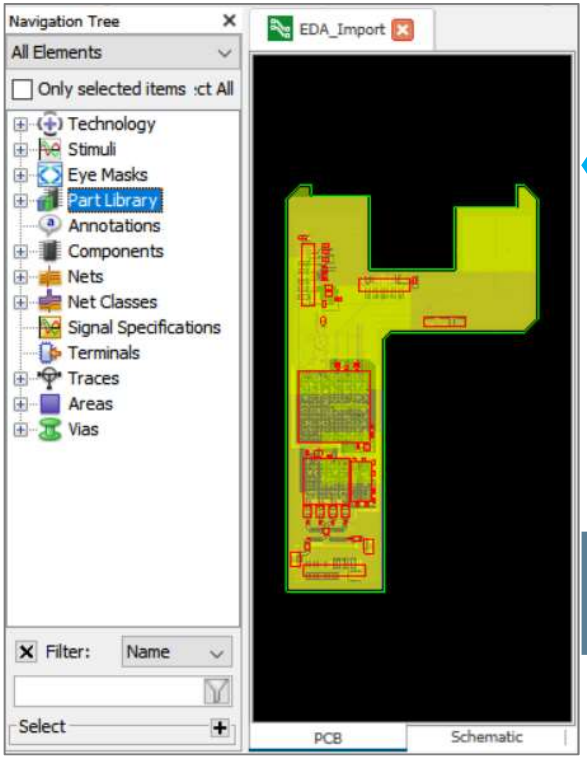
Index	Component	Power Pin	Power Net	Ground Pin	Gr...	Voltages[V]	Drop at Power Pin[V]	Drop at Ground Pin[V]	Currents[A]	Fail/Pass
0	h3	h3_36	VIN	h3_35	GND	3.69989	0.00011	0.0	0.55	
1	u1	u1_e15	1V8	u1_g15	GND	1.73746	0.06158	0.0009596	-0.1	
2	u1	u1_h12	1V8	u1_g10	GND	1.7373	0.062	0.0006957	-0.1	
3	u1	u1_j15	1V8	u1_g15	GND	1.73712	0.06192	0.0009596	-0.1	
4	u1	u1_n15	1V8	u1_p14	GND	1.73724	0.06207	0.0006863	-0.1	
5	u5	u5_45	1V8	u5_46	GND	1.7366	0.06265	0.000753	-0.05	
6	u5	u5_55	1V8	u5_46	GND	1.7366	0.06265	0.000753	-0.05	
7	u5	u5_56	1V8	u5_46	GND	1.73662	0.06263	0.000753	-0.05	



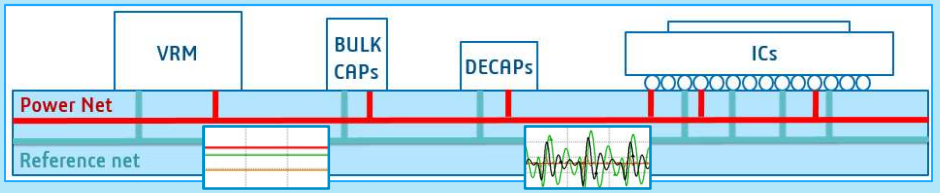
SPATIAL PLOTs

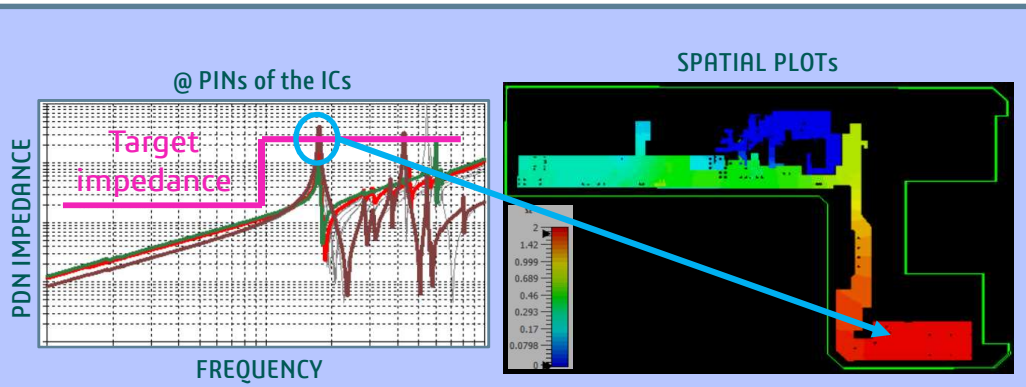


Power Integrity (HF analysis)

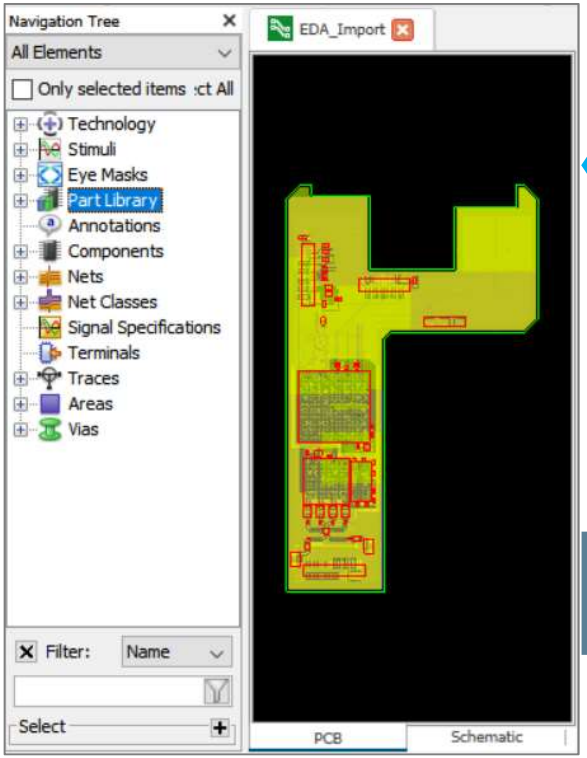


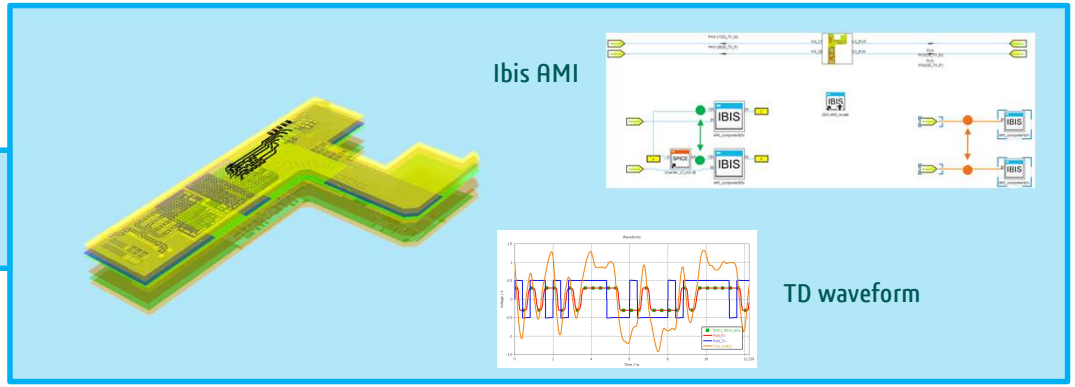
PI Analysis with IR-Drop and PI Solver:

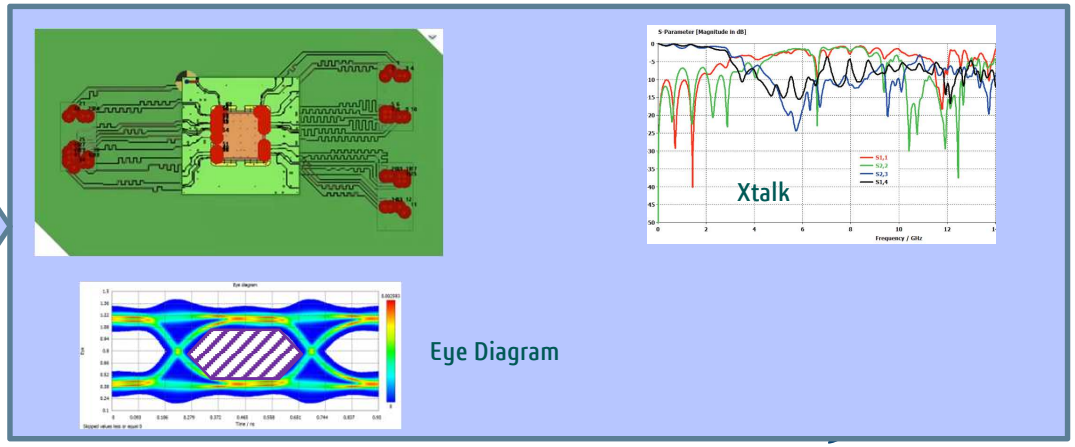




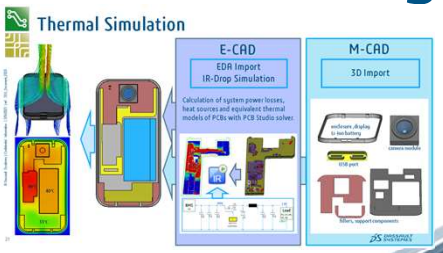
Signal Integrity

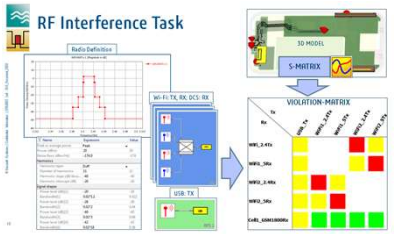


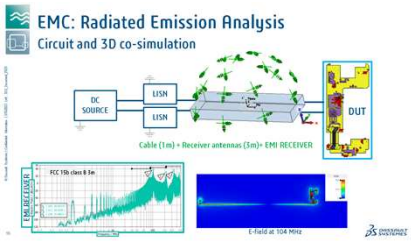


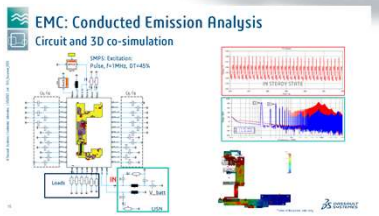


MWS Studio GUI for system analysis







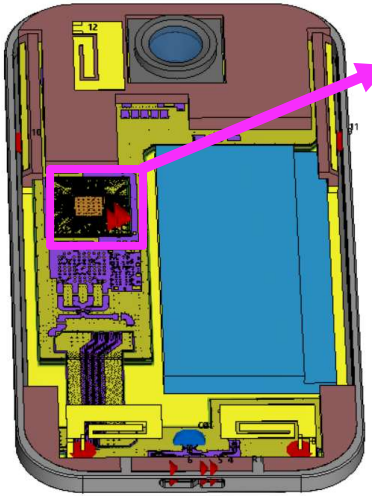


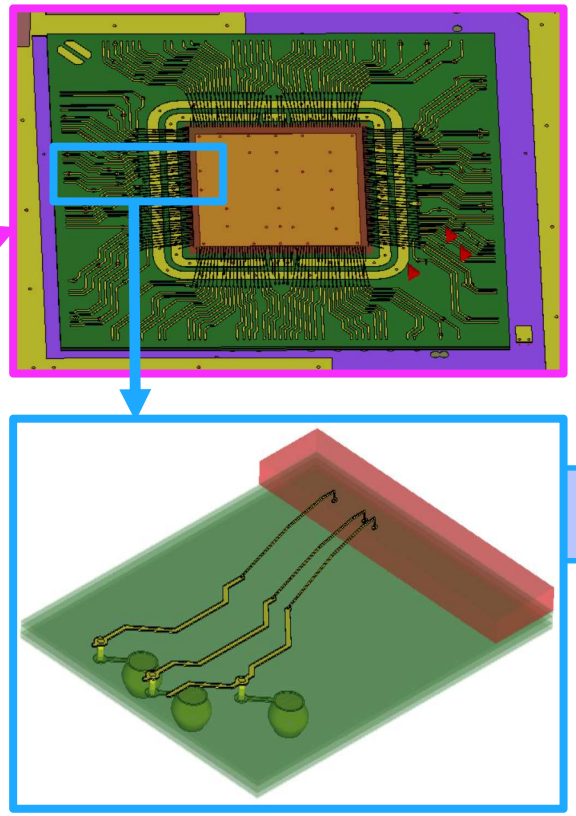
CST Studio Suite 2023

CPU or PCB import in PCB Studio GUI

DASSAULT SYSTEMES

Partial RLC Extraction





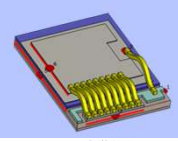
Full-wave Solvers

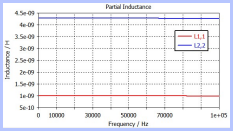
Calculation of a complete coupling matrix, including loop resistances and inductances, saved as TOUCHSTONE file.

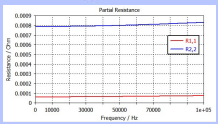
Partial RLC Solver

Partial RLC of a conductor calculated in broadband spectrum and saved into SPICE file.

Very useful for high power inverter technology







SPICE

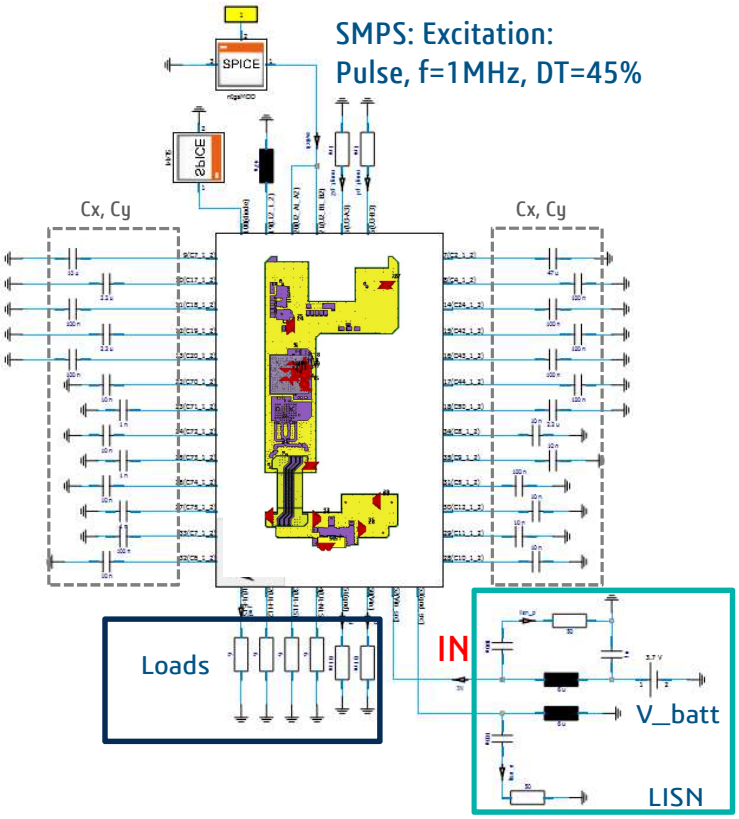
TS

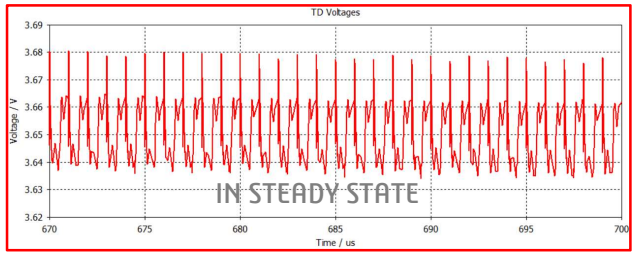
Further information:
SIMULIA Blog

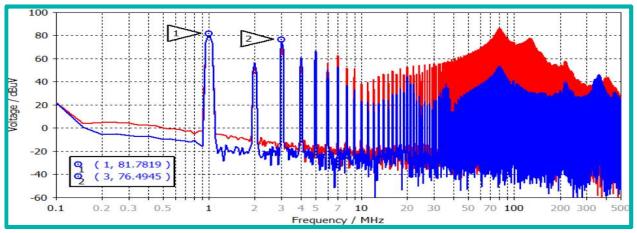
DASSAULT SYSTEMES

EMC: Conducted Emission Analysis

Circuit and 3D co-simulation



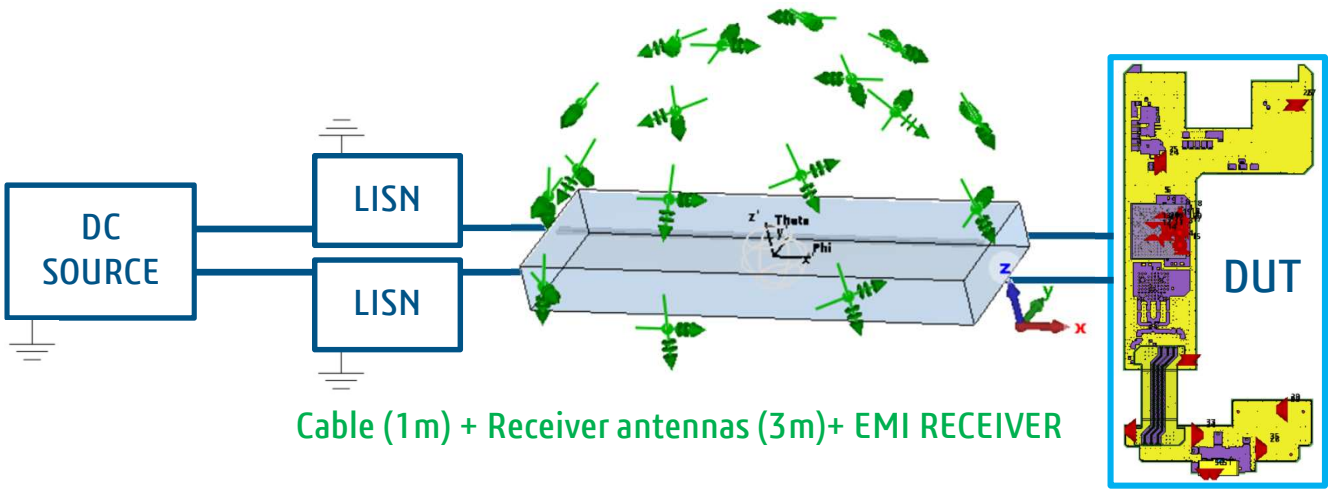




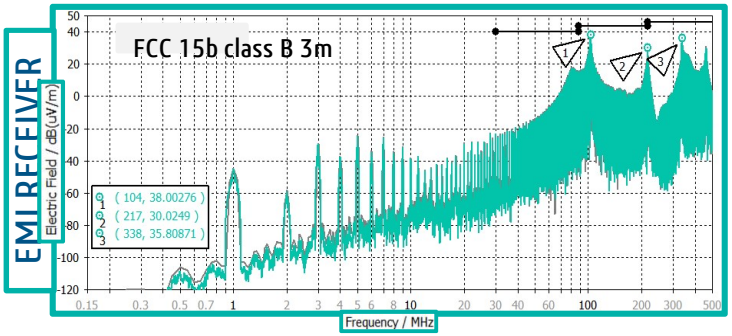
* view of the power nets only

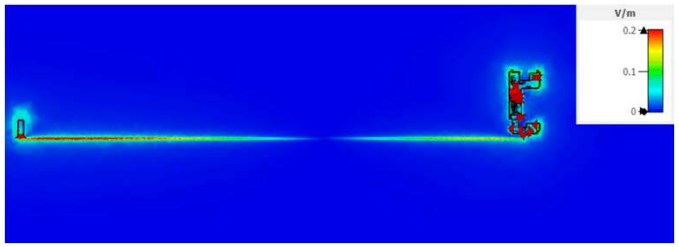
EMC: Radiated Emission Analysis

Circuit and 3D co-simulation



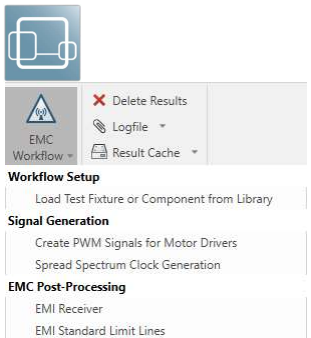
Cable (1m) + Receiver antennas (3m)+ EMI RECEIVER

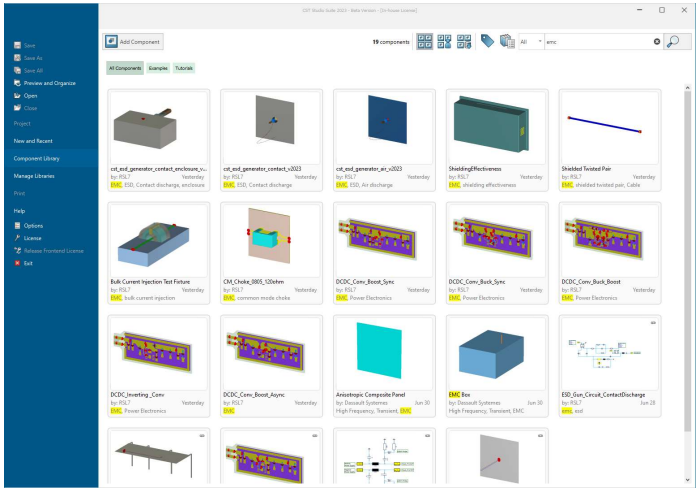


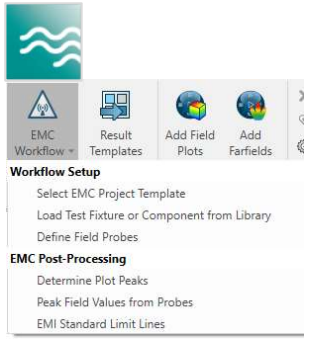


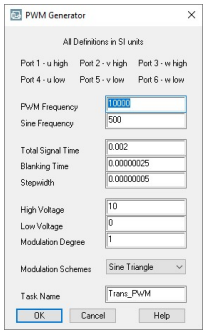
E-field at 104 MHz

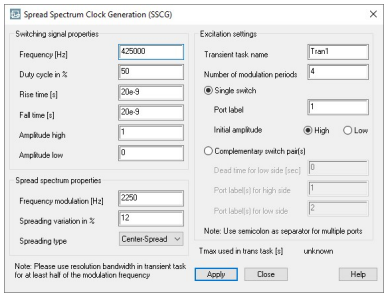
New EMC workflows button in V2023

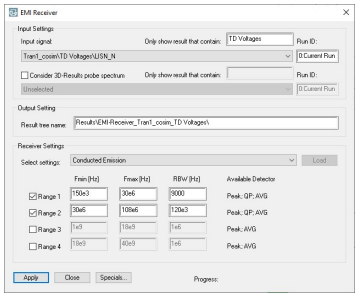


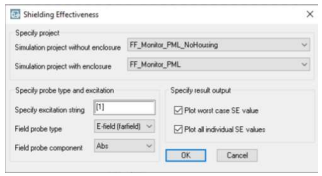


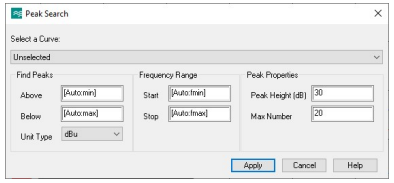


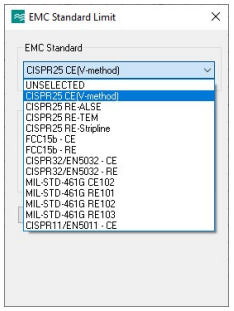




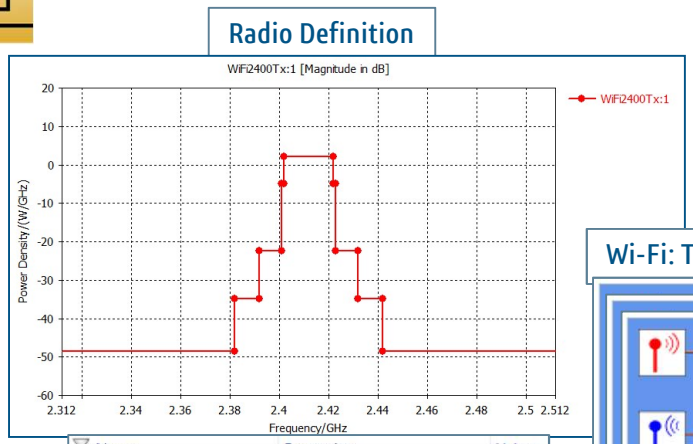




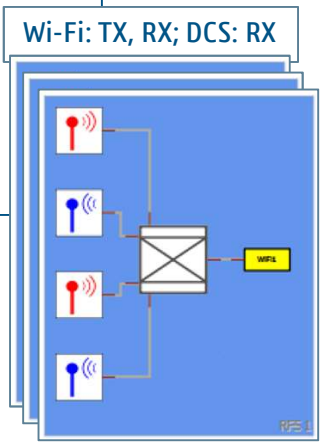


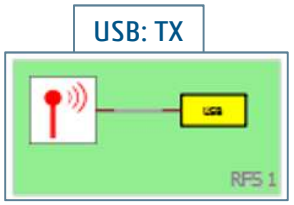


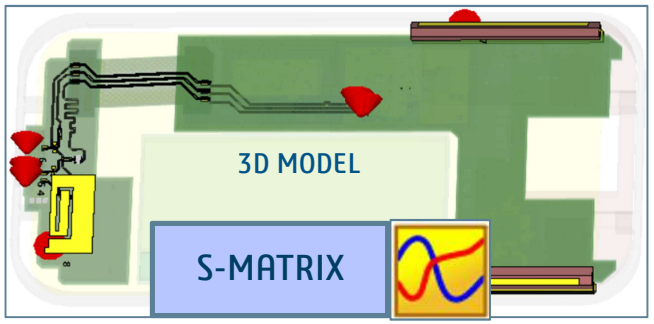
RF Interference Task

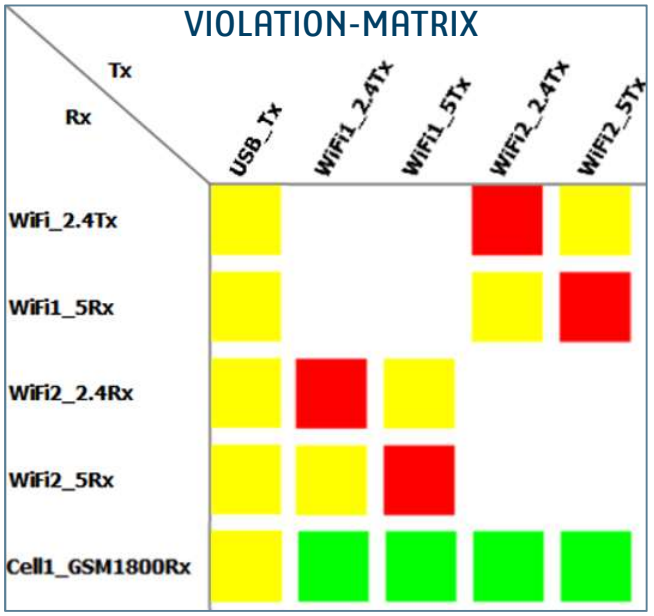


Name	Expression	Value
Peak or average power	Peak	
Power (dBm)	20	20
Noise floor (dBm/Hz)	-174.0	-174
Harmonics		
Harmonic taper	Duff	
Number of harmonics	11	11
Harmonic slope (dB/deca...	-40	-40
Harmonic intercept (dB)	-20	-20
Signal shapes		
Power level (dB)[1]	-20	-20
Bandwidth[1]	0.02*1.1	0.022
Power level (dB)[2]	-28	-28
Bandwidth[2]	0.02*2	0.04
Power level (dB)[3]	-40	-40
Bandwidth[3]	0.02*3	0.06
Power level (dB)[4]	-42	-42
Bandwidth[4]	0.02*18	0.36



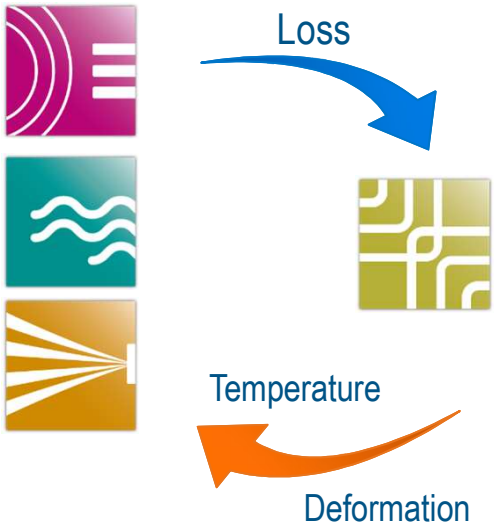






CST MPHYSICS STUDIO ®

Shared GUI
Seamless EM-MPS link



Classic Thermal

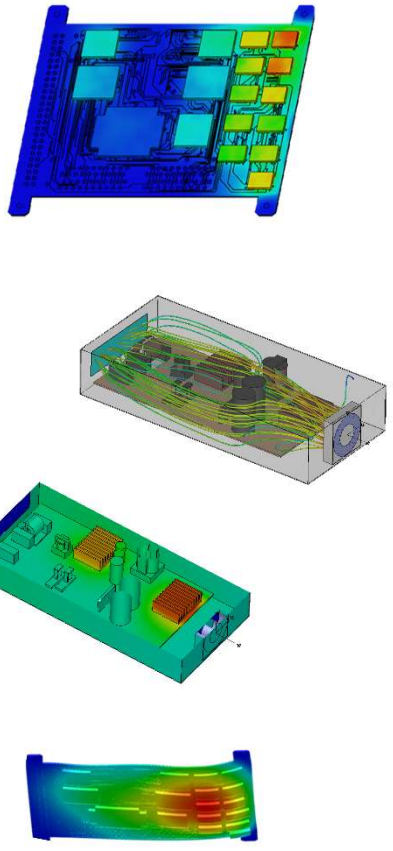
- Steady State and Transient
- Tet and Hex Meshes
- Moving Media
- Bio-heat transfer

Conjugate Heat Transfer

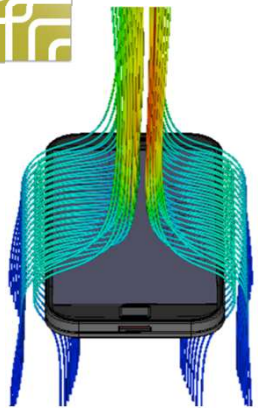
- Solve thermal conduction, convection and radiation using CFD
- Laminar and turbulent flow
- Octree meshing, GPU support
- Fan, flow resistance, compact IC model, automatic altitude correction

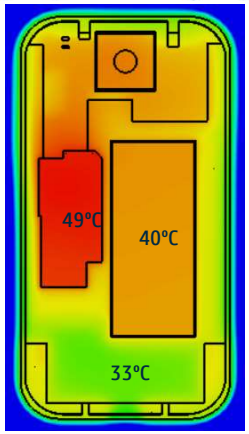
Structural Mechanics

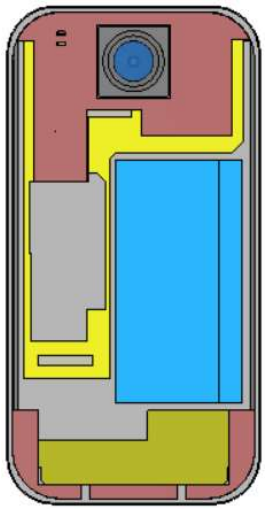
- Tet mesh, displacement, force b.c.
- Thermal stress from temp distribution



Thermal Simulation







Thermal Models

- layers
- vias
- traces
- areas

- Materials with thermal properties
  - Anisotropic thermal conductivity
  - Diffusivity
  - Material density
  - Specific heat
  - Emissivity
- Contact properties

Phone Components – 3D CAD

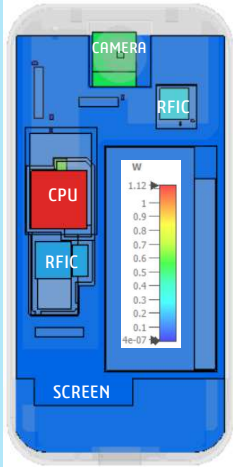
enclosure ,display
Li-Ion battery

camera module

USB port

fillers, support components

Components Heat Sources

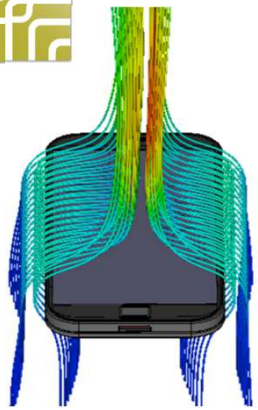


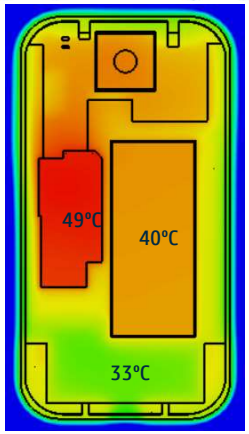
Bringing CAD data together in 3D:

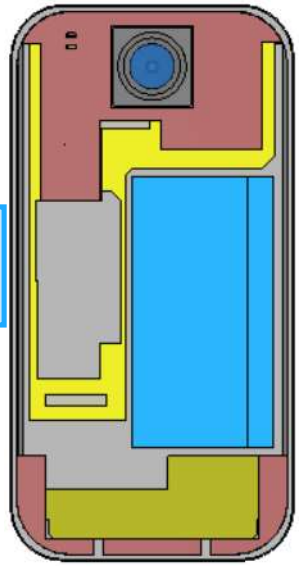
- WCS
- Anchors
- Pick tools
- Align tool

Heat Sources automatically placed on the PCBs

Thermal Simulation



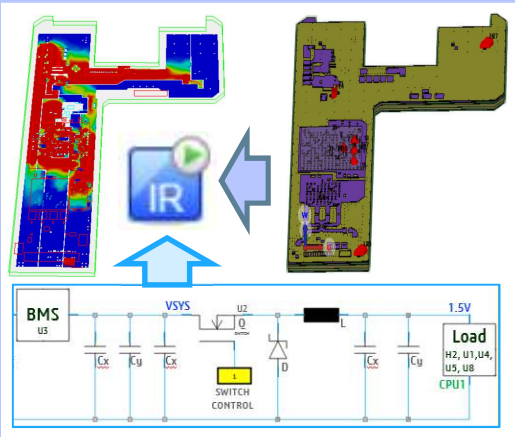




E-CAD

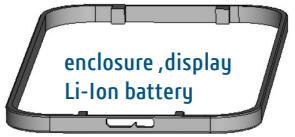
EDA Import
IR-Drop Simulation

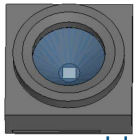
Calculation of system power losses, heat sources and equivalent thermal models of PCBs with PCB Studio solver.



M-CAD

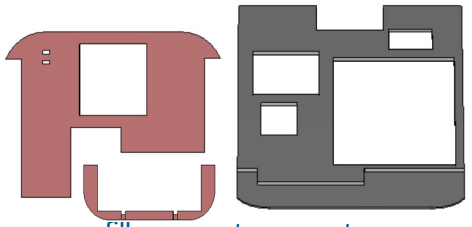
3D Import





camera module

USB port



fillers, support components

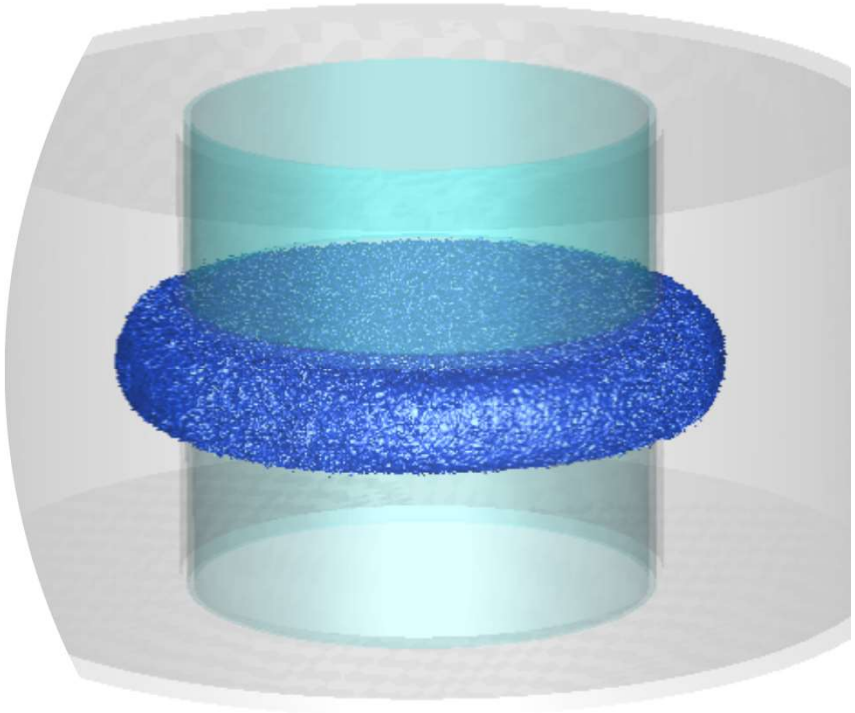
DASSAULT SYSTEMES

3DEXPERIENCE®

SEMICONDUCTOR MANUFACTURING EQUIPMENT

Richard COUSIN – Dassault Systèmes
richard.cousin@3ds.com

DASSAULT SYSTEMES | The 3DEXPERIENCE® Company



THE SEMICONDUCTOR INDUSTRY – A GROWING MARKET

- One of the most competitive Market
- Worldwide Sales > 100B$ in 2021
  - An increase of 44% compared to 2020
- Increasing Demand for IoT and Integrated Circuits
- There are needs for
  - Automation
  - Reduced Product Development Timelines
- But this requires
  - An Increasing development & Fabrication costs
  - Innovation & Competitive developments

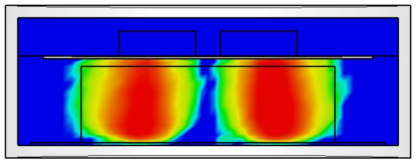
- **The Simulation tools at the Fabrication process level can help facing those challenges**

THE SEMICONDUCTOR MANUFACTURING PROCESS

Plasma for Semiconductors

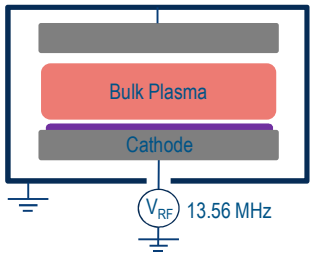
Plasma Modelling

- High Prediction of Electron/Ion Density Profiles
- Control of Plasma homogeneity
- Etching Process Quality

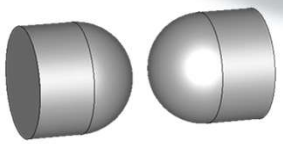


Wafer Manufacturing

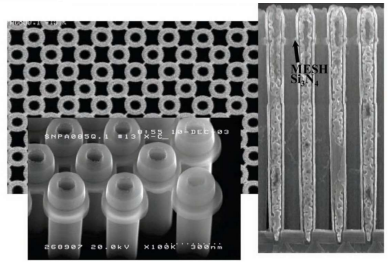
Type of Reactor Design (CCP/ICP)



Low Pressure Discharge



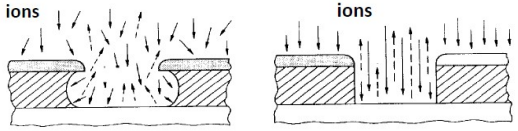
Type of Semiconductors and choice of materials



[Samsung, sub-70nm DRAM, 2004]

Selection of the Dry Etching Process (Plasma Exposure)

- Pressure range
- Plasma Density
- Isotropic vs Anisotropic Etching Process

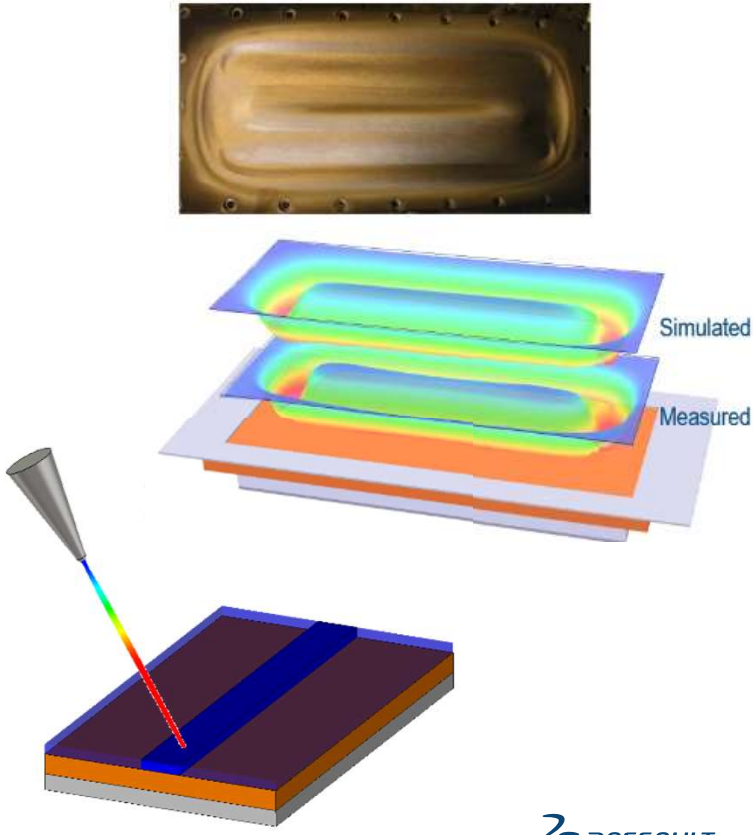


SIMULIA

DASSAULT SYSTEMES

A SET OF SEVERAL PROCESSES ON DEMAND

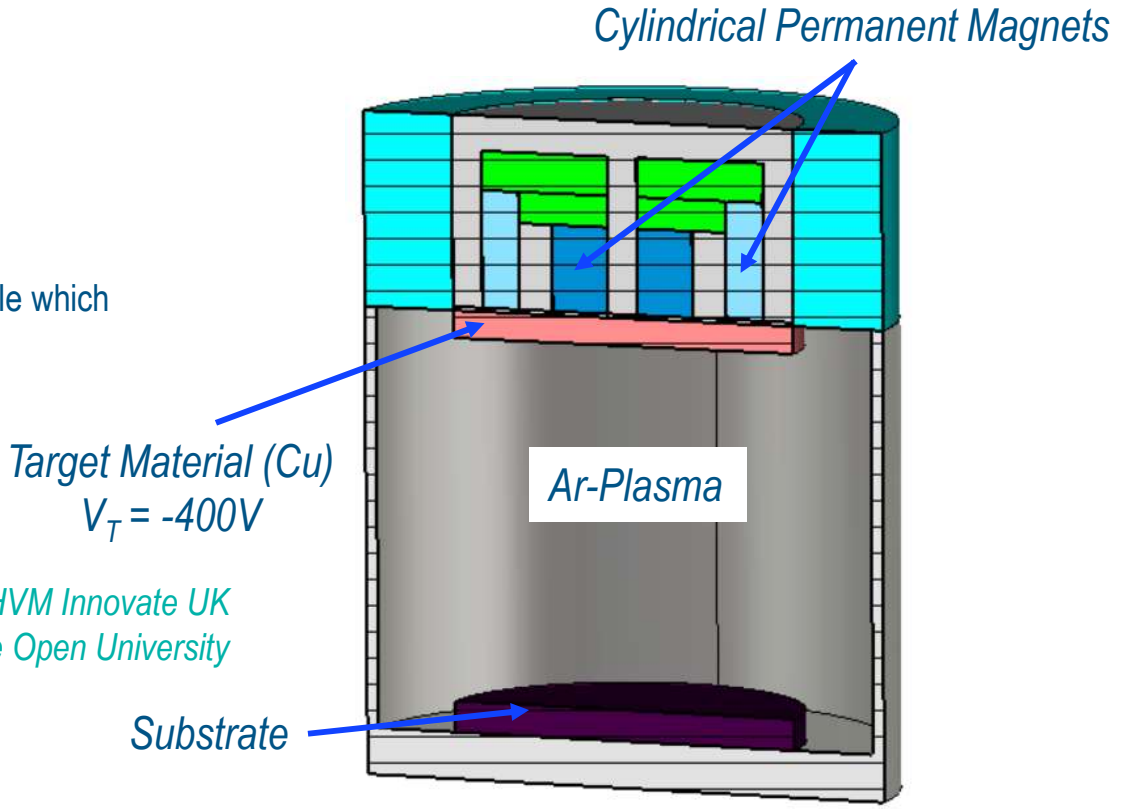
- **Thin Film Deposition**
  - DC/RF Sputtering
- **Etching Process**
  - Dry Plasma Etching (Physical & Chemical)
  - CCP/ICP
- **Doping Process**
  - Ion Implantation
- **Lithography**
  - E-beam Lithography – To create the masks for Extreme UV Photo-lithography
  - Sintering Printed Circuits for Flexible Electronics



THIN FILM DEPOSITION THE DC-MAGNETRON SPUTTERING

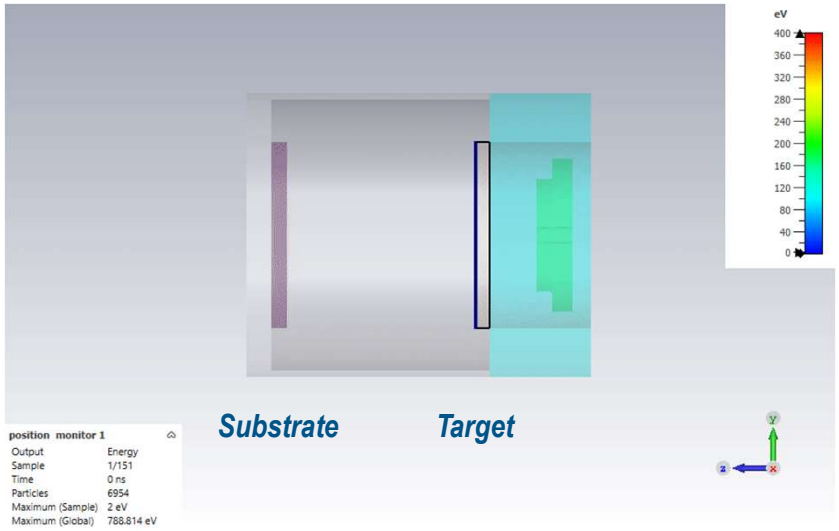
DC-MAGNETRON SPUTTERING EXAMPLE

- Target Voltage @ -400V to trap the ions
- Pressure range from 1 to 5 mTorr
- Target Materials usually made of Al, Cu, Ti
- Target thicknesses from 1 to 3 mm
- The Goal is to estimate the target erosion profile which would affect the long term sputtering efficiency

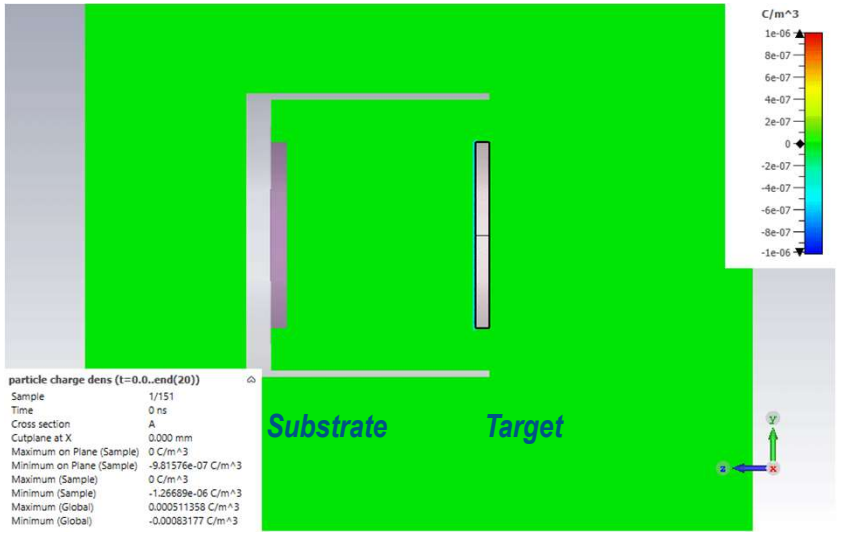


Ref: Magnetron data courtesy of the MOMS4HVM Innovate UK project involving Teer Coatings and The Open University

PLASMA IGNITION – TRANSIENT BEHAVIOR



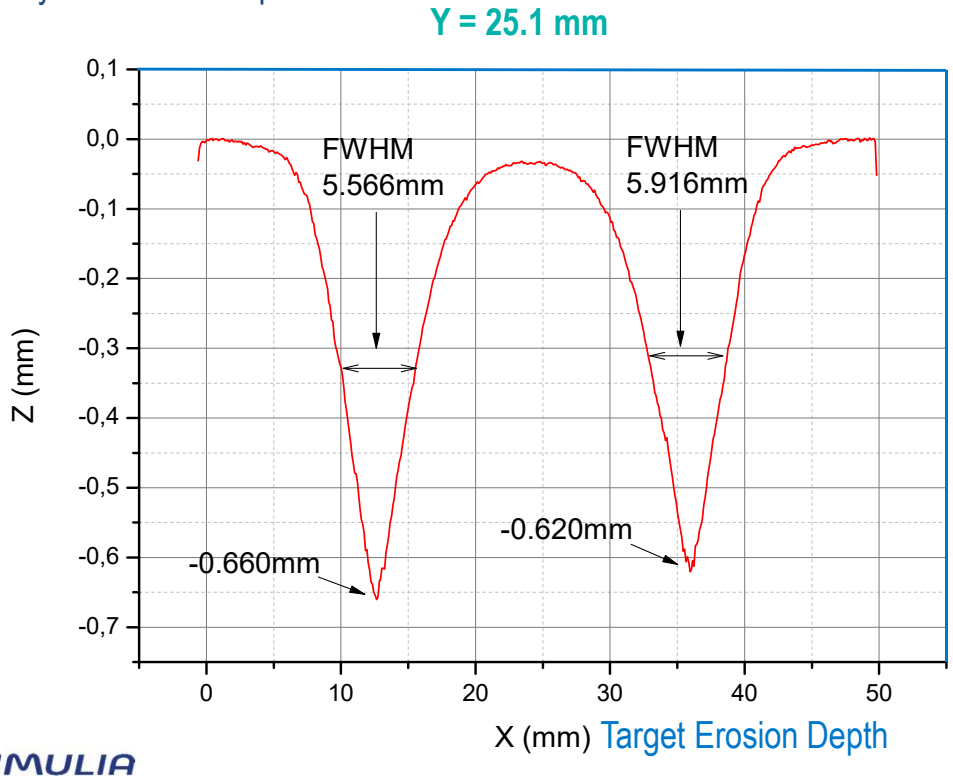
Plasma Expansion and Particle energy concentration at the Target surface



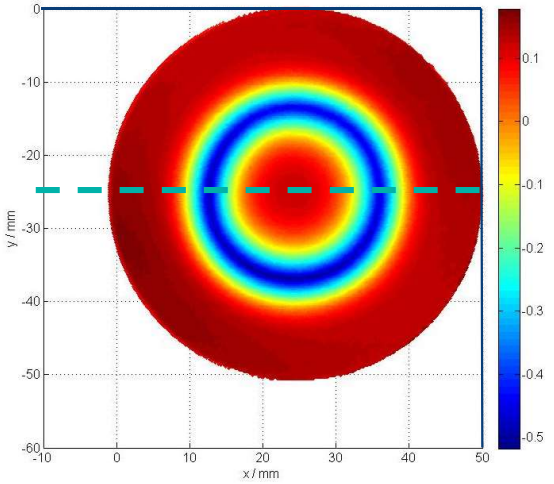
Electron & Ion beam Profiles with evidence of Ar-Ion bombardments on the Target surface

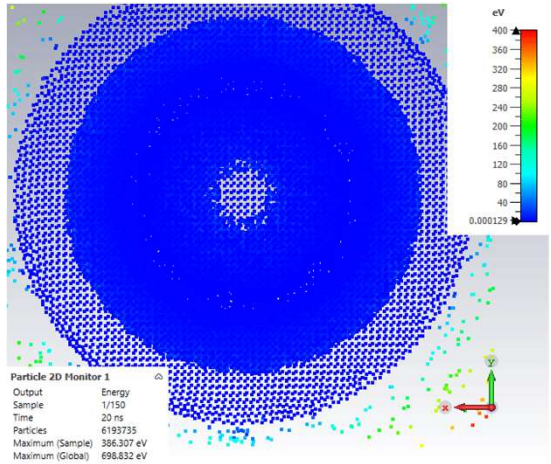
TARGET EROSION PROFILE PREDICTION

- Increased erosion depth at X=12mm, X=36mm due to local maximum of plasma density and ionization profile



Target Erosion Depth



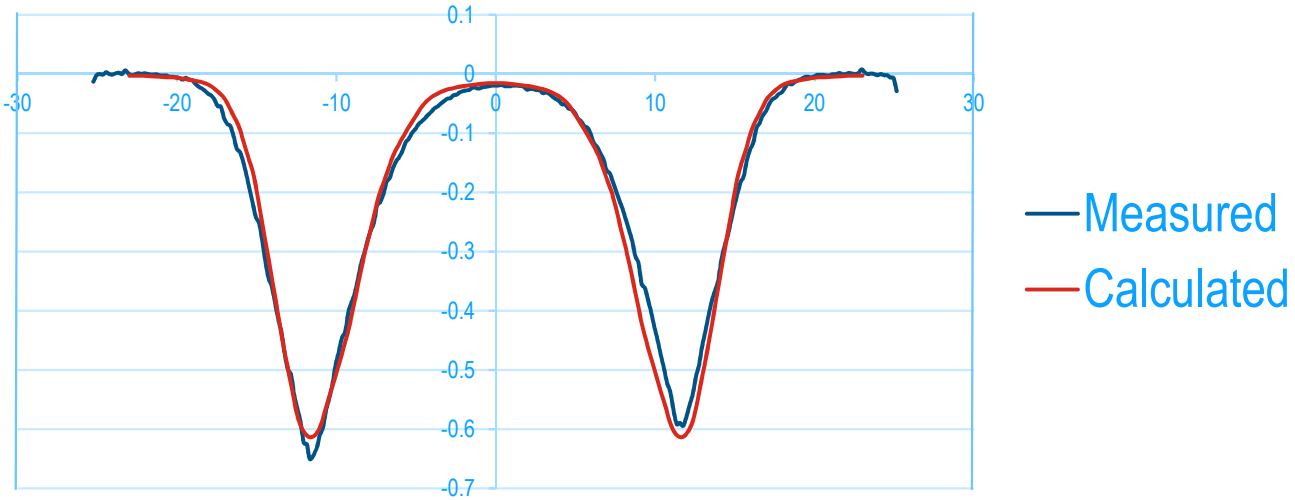


SIMULIA

DASSAULT SYSTEMES

SIMULATION PREDICTION – VIRTUAL PROTOTYPING

- Erosion grove Depth for a Cu-Target
- Target thickness of 3 mm
- Pressure of 1mTorr
- Very good prediction of the target erosion Profile – The simulation tools can be used for further virtual prototyping



Ref: Measurements performed at the Open University (UK)

SUMMARY & CONCLUSIONS

BENEFITS OF USING SIMULATION

High Fidelity modeling to predict/explain experimental results when no diagnostics are available

Reduced cost by optimizing device performance and reliability

- Prediction of potential damage

Accelerate device validation and decision for the right Semiconductor Manufacturing Processes

CONCLUSION: A UNIQUE VALUE PROPOSITION

Exploring New Plasma Reactor Designs

- ▷ A Unique 3D Plasma Modelling
- ▷ Time Domain Approach and Charged Particle Dynamics computation
- ▷ GPU support

Adaption of Existing Equipment to the New Technologies

- ▷ Design Modification and Traceability
- ▷ Prediction of potential damage

A Complete Technology

- ▷ Large choice of solvers and meshing techniques
- ▷ Multi-Physics approach – Thermal coupling analysis possible

DASSAULT SYSTEMES